ABSTRACT OF THE DISCLOSURE

A decoding circuit used to correct an error in a digital signal comprises: an input unit for entering coded digital signals ID in parallel in accordance with the number of interleaved codes; a processor including an error locator polynomial calculator and an error value polynomial calculator for processing data obtained serially from the interleaved codes that are received by the input unit; and an output unit for correcting errors by employing the output data that are received from the processor and the digital signals ID, and for outputting in parallel the obtained digital signals OD, for which an error has been corrected by a linear calculation on a Galois field, in accordance with the number of interleaved codes.